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10/830,068	04/23/2004	Young Joon Ahn	YHK-0135	7680

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KED & ASSOCIATES, LLP
P.O. Box 221200
Chantilly, VA 20153-1200

EXAMINER	
GUHARAY, KARABI	
ART UNIT	**PAPER NUMBER**
2879	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/830,068	AHN, YOUNG JOON	
	Examiner	Art Unit	
	Karabi Guharay	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Amendment, filed on 2/13/07*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5,7-9,11-13,26-37 and 39-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5,7-9,11-13,26-37 and 39-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/27/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment

Translation of foreign priority document, filed on 2/13/2007 has been considered and entered.

Outstanding rejection of claims 26, 30 and 41 are withdrawn in light of translation of foreign priority document.

The indicated allowability of claims previously presented are withdrawn in view of the newly discovered reference to Chang (US 20030102803). Rejections based on the newly cited reference follow.

Claim Objections

Claim 33 is objected to because of the following informalities: Claim 33 depends from claim 1, which recites "buffer layer or dielectric layer". So in the structure there will be either a buffer layer or a dielectric layer, and there is no separate layer, while claim 33 recites both buffer layer and dielectric layer which is different from buffer layer. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 32, 36-37 & 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Ebihara et al. (US 6514111).

Regarding to claims 32, 37 & 42, Ebihara discloses in Figures 1, 2A-C and 5A-C, a plasma display comprising: a first substrate (220); a second substrate (270) arranged with respect to the first substrate (220) such that a discharge space is provided therebetween; a sealing layer (320) between the first substrate (220) and the second substrate (270); at least one of a buffer layer (240) or a dielectric layer provided on the first substrate (220) and provided between the first substrate (220) and the sealing layer (320); wherein the buffer layer has a thickness (240) has a thickness of 35 Micron to 50 micron between the sealing layer and the first substrate (lines 49-58 of column 8) and a protective layer (260) on the dielectric layer and further comprising plurality of electrodes (23, 230) on the first substrate .

Regarding to claim 36, Ebihara discloses in Figures 1 and 2A-C, the at least one of the buffer layer (24a) or the dielectric layer is the buffer layer (24a), and the dielectric layer (25) is formed on the buffer layer (24a) such that the buffer layer (24a) is provided between the first substrate (22) and the dielectric layer (25) and such that the dielectric layer (25) is provided between the buffer layer (24a) and the protective film (26).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 5, 7-9, 11, 26, 33-35, 40-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Us Patent No. 6,514,111, and further in view of Chang (US 20030102803).

Regarding to claims 1, 9, 26 & 40-41, Ebihara discloses in Figures 1 and 2A-2C, a plasma display panel (1), comprising: a first substrate (22); a second substrate (27) facing the first substrate (22) with a discharge space therebetween; a sealing layer (32) located between the first substrate (22) and the second substrate (27); and at least one of a buffer layer (24a) or a dielectric layer formed between the first substrate (22) and the sealing layer (32); and a protective film (26) formed on the at least one of the buffer layer (24a) or the dielectric layer.

Ebihara further discloses the buffer or dielectric layer (24) is formed by a low-melting-point glass paste mainly comprising PbO (see column 4, lines 27-38).

However, Ebihara does not specifically disclose the detailed composition of the dielectric layer as claimed.

The Chang reference teaches a plasma display panel, having a dielectric layer(100 of Fig2) composed of PbO at a ratio of 45% to 55%, B203 at a ratio of 10% to 20% and SiO2 at a ratio of 15% to 25% (see Table 1 of paragraph 41) and the dielectric layer having a thermal expansion coefficient of approximately 72 $X10^{-7}$ – $86X10^{-7}$/° C (see paragraph 45), for the purpose of enhancing contrast of the display by controlling light transmittance of visible light by the dielectric layer (see Abstract).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have utilize the dielectric layer of Chang for the plasma display panel of Ebihara in order to effectively increase the contrast of the display.

Regarding to claim 3, Ebihara discloses in Figures 1 and 2A-C, the buffer layer (24a) is formed by a low-melting-point glass paste mainly comprising lead oxide (see column 4, lines 27-38) and the first substrate (22) is made of glass which is a different material from that of the buffer layer and thus a range of thermal expansion coefficient of the buffer layer is different from a range of thermal expansion coefficient of the first substrate.

Regarding to claim 5, albeit, Ebihara discloses the buffer layer and the sealing layer both comprises mainly of PbO, however, Ebihara specifically discloses the buffer layer having a softening point of 580°C (see column 6, lines 41-53) and the sealing layer having a softening point of 400°C (see column 7, lines 37-48) and thus, the buffer layer and the sealing layer may comprises of the same material however with different component compositions. Therefore, a range &thermal expansion coefficient of the buffer layer is different from a range of thermal expansion coefficient of the sealing layer.

Regarding to claim 7, the thermal expansion coefficient of the first substrate is merely a property of the material used in manufacture the first substrate, and the property of the material does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations and thus this limitation has not given

patentable weight.

Regarding to claim 8, the thermal expansion coefficient of the sealing layer is merely a property of the material used in manufacture the sealing layer, and the property of the material does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations and thus this limitation has not given patentable weight.

Regarding to claim 11, Ebihara discloses in Figures 1 and 2A-C, the dielectric layer (25) and the buffer layer (24a) such that the buffer layer (24a) is provided between the first substrate (22) and the dielectric layer (25) and such that the dielectric layer (25) is provided between the buffer layer (24a) and the protective film (26).

Regarding to claim 33, Ebihara discloses in Figures 1 and 2A-C, the buffer layer (24a) is different than the upper dielectric layer (25).

Regarding claim 34 & 35, Ebihara et al. disclose all the limitations of claims 34 & 35 (see rejection of claim 32 above) except for the claimed composition of the dielectric layer and claimed thermal expansion coefficient of the dielectric layer.

However, the Chang reference teaches a plasma display panel, having a dielectric layer (100 of Fig 2) composed of PbO at a ratio of 45% to 55%, B203 at a ratio of 10% to 20% and SiO2 at a ratio of 15% to 25% (see Table 1 of paragraph 41) and the dielectric layer having a thermal expansion coefficient of approximately 72 $X10^{-7}$ – $86X10^{-7}/^{o}$ C (see paragraph 45), for the purpose of enhancing contrast of the display by controlling light transmittance of visible light by the dielectric layer (see Abstract).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have utilize the dielectric layer of Chang for the plasma display panel of Ebihara in order to effectively increase the contrast of the display.

Claims 26-28, 30, 31and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,495,262 to Igeta in view of Chang (US 2003/0102803).

Regarding to claims 26 & 39, Igeta discloses in Figures 1-4, a plasma display panel, comprising: a first substrate (1B); a second substrate (1A) arranged with respect to the first substrate (1B) such that a discharge space is provided therebetween; a sealing layer (22a) between the first substrate (1B) and second substrate (1A); and at least one of a buffer layer (22b) or dielectric layer formed between the first substrate (1B) and the sealing layer (22a).

However, Igeta does not disclose the at least one of the buffer layer or the dielectric layer has a thermal expansion coefficient greater or equal to 72xl 0"7/°C.

The Chang reference teaches a plasma display panel, having a dielectric layer(100 of Fig 2), composed of PbO at a ratio of 45% to 55%, B203 at a ratio of 10% to 20% and SiO2 at a ratio of 15% to 25% (see Table 1 of paragraph 41) and the dielectric layer having a thermal expansion coefficient of approximately 72 $X10^{-7}$ – $86X10^{-7}$/° C (see paragraph 45), for the purpose of enhancing contrast of the display by controlling light transmittance of visible light by the dielectric layer (see Abstract).

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have utilize the dielectric layer of Chang for the plasma display panel of Igeta in order to effectively increase the contrast of the display.

Regarding to claim 27, Igeta discloses in Figures 1-4, the sealing layer (22a) extends in a longitudinal direction (vertical direction) from a first end to a second end, the first end located proximal to the first substrate (1B) and the second end located proximal to the second substrate (1A), the buffer layer (22b) provided only in the area between the first end of the sealing layer (22a) and the first substrate (1B).

Regarding to claim 28, Igeta discloses in Figures 1-4, another sealing layer (22a on the opposite end thereof) between the first substrate (1B) and the second substrate (1A); and another buffer layer (22b on the opposite end thereof) formed between the first substrate (| B) and the another sealing layer (22a on the opposite end thereof) such that the another buffer layer (22b on the opposite end thereof) is provided only in another area between the first substrate (1B) and the another sealing layer (22a on the opposite end thereof), the another buffer layer (22b on the opposite end thereof) to compensate thermal stress of the first substrate (1B) and the another sealing layer (22a on the opposite end thereof).

Regarding to claim 30, Igeta discloses in Figures 1-4, a thermal expansion coefficient of the buffer layer (2B of 22b) is different from a thermal expansion coefficient of the first substrate (1B).

Regarding to claim 31, Igeta discloses in Figures 1-4, a thermal expansion coefficient of the buffer layer (2B of 22b) is different from a thermal expansion coefficient of the sealing layer (2A of 22a).

Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,514,111 to Ebihara of record in view of Chang (U.S 2003/0102803), and further in view of U.S. Patent No. 6,261,144 to Nishiki of record.

Regarding to claim 12, Ebihara in view of Kawana discloses in Figures 1 and 2A-2C, a plasma display panel (1), comprising: a first substrate (22); a second substrate (27) facing the first substrate (22) with a discharge space therebetween; a sealing layer (32) located between the first substrate (22) and the second substrate (27); and at least one of a buffer layer (24a) or a dielectric layer formed between the first substrate (22) and the sealing layer (32); wherein the at least one of the buffer layer or the dielectric layer includes the following composition: PbO at a ratio of 45% to 55%, B203 at a ratio of 10% to 20% and SiO2 at a ratio of 15% to 25%; and a protective film (26) formed on the at least one of the buffer layer (24a) or the dielectric layer.
However, Ebihara and Chang do not disclose that the buffer layer is formed to be extended from the dielectric layer.
The Nishiki reference teaches in Figure 7A, a plasma display panel having an upper dielectric layer (18) formed on the first substrate (14) and the buffer layer is formed to be extended from the upper dielectric layer (18) for the purpose of efficiently sealing of

the plasma display panel.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have utilize the buffer layer of Kawana and the buffer layer extended from the upper dielectric layer of Nishiki for the plasma display panel of Ebihara in order to efficiently seal the plasma display panel.

Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,495,262 to Igeta of record in view of Chang (US 2003/0102803), further in view of U.S. Patent No. 6,514,111 to Ebihara of record.

Regarding to claim 29, Igeta in view of Chang disclose all the limitations of claim 29 (see rejection of claim 28) except for the limitation of plasma display panel comprising an upper dielectric layer formed on the first substrate between the buffer layer and the another buffer layer; and a protective film formed on the upper dielectric layer (25) for the purpose of reducing the stress in the dielectric layer of the sealing region, there by the occurrence of flaws therein is avoided without reducing the thickness of the dielectric layer in the display region.

Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have utilize buffer layer of Chang and the upper dielectric layer and a protective film of Ebihara for the plasma display panel of Igeta in order to reduce the stress in the dielectric layer of the sealing region, there by the occurrence of flaws

therein is avoided without reducing the thickness of the dielectric layer in the display region.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Karabi Guharay whose telephone number is 571-272-2452. The examiner can normally be reached on Monday-Friday 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar D. Patel can be reached on 571-272-2457. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

K Guharay

Karabi Guharay
Primary Examiner
Art Unit 2879
5/7/07